i.MX 7ULP

SESIP Security Target

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Document information

Information	Content
Keywords	SESIP, Security Target, i.MX 7ULP
Abstract	Evaluation of the i.MX 7ULP developed and provided by NXP Semiconductors, BL MICR, according to SESIP Assurance Level 1 (SESIP1)

Revision History

Rev.	Date	Description
1.0	2018-02-20	First version
1.1	2018-02-20	Small correction of SFRs for i.MX 7ULP platform
1.2	2018-02-25	Update after evaluator comments

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1   Introduction

This Security Target describes the i.MX 7ULP platform that is evaluated according to the Security Evaluation Scheme for IoT Platforms (SESIP) [1]. The security properties are described in Section 3 of this document, and will be uphold by the platform when the objectives for the environment (described in Section 2) are fullfilled by the platform consumer.

1.1   ST Reference

i.MX 7ULP, SESIP Security Target, Revision 1.2, NXP Semiconductors, 25 February 2019.

1.2   TOE Reference

Table 1. TOE Reference

Reference	Value
TOE Name	i.MX 7ULP
TOE Version	Rev. A and Rev. B
TOE Identification	i.MX 7ULP
TOE Type	Microcontroller platform for connected applications

Note: The difference between TOE Version Rev. A and Rev.B are optimalizations only. There is no difference in security functionality between the revisions.

1.3   Guidance Documents

The following documents are included with the platform:

Table 2. Guidance Documents

Document	Reference
Reference Manual	i.MX 7ULP Applications Processor Reference Manual 2.0, NXP Semiconductors, Document Number: IMX7ULPRMV2 [2]
Security Reference Manual	i.MX 7ULP 2.0 Security Reference Manual, NXP Semiconductors, Document Number: IMX7ULPSRMV2 [3]

1.4   TOE Overview and Description

The i.MX 7ULP processor represents NXP's latest achievement in ultra-low-power processing for use cases demanding long battery life. Targeted towards the growing market of portable devices, the i.MX 7ULP family of processors features NXP's advanced implementation of the Arm® Cortex®-A7 core, the Arm Cortex-M4 core, as well as a 3D and 2D Graphic Processing Units (GPUs). The i.MX 7ULP provides up to 32-bit LPDDR2/LPDDR3 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors.

Its main features are:

- Cortex-A7 @ 500MHz/800MHz
- Cortex-M4 @ Nominal150Mhz
- 256 KB L2 cache

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- Total of 512 KB of on-chip RAM
- 16-/32-bit LPDDR2/3
- Full security w/ tamper resist
- Separate system power domains with IPC

Memory options

- QSPI, 32 bit LPDDR2/3, eMMC 5.0 /SD3.0

The functional block diagram is shown in the figure below. This diagram provides a view of the chip's major functional components and core complexes.
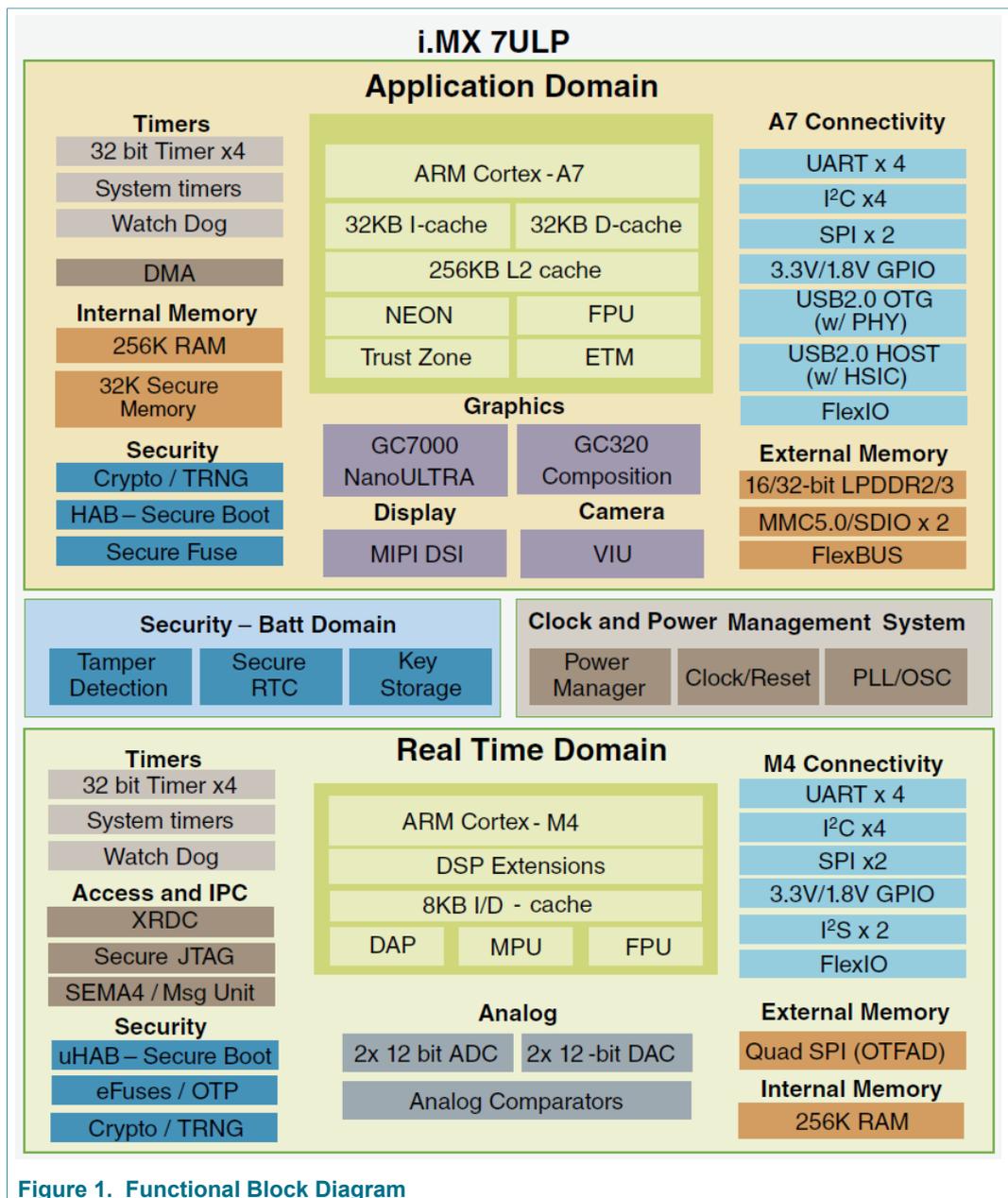

Figure 1. Functional Block Diagram

The platform consists of a microcontroller implementing High Assurance Boot, support for cryptographic primitives AES-128/256, SHA-1, SHA-224, SHA-256, random number generation, support of tamper detection and more.

The platform is intended to be used by an integrator that deploys it into a connected solution together with its own operating systems and user applications.

The main security features of the platform are listed in Section 3 of this document.

1.4.1 Physical Scope of the TOE

The physical scope is the i.MX 7ULP microcontroller as identified in Table 1 and whose functional blocks are identified in Figure 1. It includes the dedicated firmware located in the on-chip boot ROMs.

1.4.2 Logical Scope of the TOE

The logical scope includes the hardware interfaces that operating systems or applications would make use of. The logical scope of the firmware is limited to the uHAB functionality stored in the on-chip boot ROMs.

Figure 1 shows that the i.MX 7ULP provides two execution domains called Application Domain (AP) and Realtime Domain (RT). Both domains include an independent boot ROM implementing the HAB feature.

Any OS or application software stored on the platform is not in scope of this evaluation.

1.4.3 Required non-TOE Hardware/Software/Firmware

No additional non-TOE hardware, software or firmware is required for the correct functioning of the security claims described in this document.

2   Security Objectives for the Operational Environment

In order for the platform to fulfill its security requirements, the operational environment (technical or procedural) must fulfil the following objectives:

• The OS or application developer shall verify the correct version of all platform components it depends on as described in the Reference Manual

• The OS or application developer is expected to enable the uHAB feature as described in the Security Reference Manual.

• To allow execution of unknown code while maintaining the protection of platform security features as declared in Section 3, the OS or application developer shall configure restrictive memory boundaries via the MPU and shall dedicate one of the available execution domains to the security services as described in the Security Reference Manual.

Please refer to Section 1.3 for references to the guidance documentation mentioned above.

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3 Security Requirements

3.1 Security Functional Requirements

The Security Functional Requirements (SFRs) are listed below, together with a short rationale explaining why the platform meets the requirement (*in italics*).

3.1.1 Identification and Attestation of Platforms and Applications

3.1.1.1 Identification of Platform Type

The platform provides a unique identification of the platform type, including all its parts and their versions.

The chip includes values in the fuses that uniquely identify the platform type, including a part of the Lot identifier and a Silicon Revision Number as described in the Reference Manual *and* Security Reference Manual.

The fuses are written as part of the production process, and the production testing procedures verify the value has been written correctly.

3.1.1.2 Identification of Individual Platform

The platform provides a unique identification of that specific instantiation of the platform, including all its parts and their versions.

The chip includes in fuses a 64-bit unique identifier. It also includes values in the fuses that uniquely identify a lot, wafer and x-y coordinates that uniquely identify a given die.

The fuses are written as part of the production process, and the production testing procedures verify the value has been written correctly.

3.1.1.3 Secure Initialization of Platform

The platform ensures its authenticity and integrity during the platform initialization. If the platform authenticity or integrity cannot be ensured, the platform will go to a secure state.

The chip includes NXP's High Assurance Boot (HAB). When the device boots, the execution starts in the device's physical ROM by the secure boot mechanism that verifies the authenticity of the firmware before executing it. The signature uses RSASSA-PKCS1-v1_5 signature [8] *of a SHA256 digest with 1024-bit to 4096-bit key size.*

The public key used for signing the firmware is itself authenticated by a chain of signatures in a certificate, using one of four root keys. A fingerprint of these root keys is stored in the device's manufacturer-programmable on-chip fuses, and used to validate the root key.

In case of failure, depending on lifecycle and configuration, the chip may first look for a recovery boot image, before waiting on a Serial Downloader (e.g., on USB) for an authenticated image.

The HAB feature is tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.2 Product Lifecycle: Factory Reset / Install / Update / Decomission

3.1.2.1 ~~Secure Update of Platform~~

~~The platform can be updated to a newer version in the field such that the integrity, authenticity and confidentiality of the platform is maintained.~~

The platform does not support the update or patching of firmware located in the on-chip ROM. It does offer a feature for customers to implement secure update mechanisms of their own code. According to [1] the absence of this functionality for the platform must be explained as part of ALC_FLR.2. Please see Section 3.2.1 for this explanation.

3.1.2.2 Decommission of Platform

The platform can be decommissioned.

The chip includes a Field Return mode, in which access to the device keys is permanently disabled, including access from the CAAM module. In that mode, debugging is possible, as well as execution of any firmware.

The switch to Field Return mode can only be obtained by loading a chip-specific boot image that includes the chip's unique ID, verifying its authenticity, and by running it. Such a boot image can only be authenticated by using one of the keys allowed to sign firmware images.

The Field Return mode is tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.3 Extra Attacker Resistance

3.1.3.1 Software Attacker Resistance: Isolation of Platform

The platform provides isolation between the application and itself, such that an attacker able to run code as an application on the platform cannot compromise the other functional requirements.

The platform provides isolation between different kinds of applications, through the following mechanisms:

- *The device implements two separate execution domains AP and RT.*
- *The device also supports hardware-based isolation on the AP domain by combining the TrustZone technology with an Extended Resource Domain Control (XRDC) that can restrict the access to security peripherals to code running in Secure and/or privileged mode.*
- *The device also includes a MPU in the RT domain that allows another separation between Handler and Thread modes on that CPU.*

The isolation mechanisms and MPU are tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.4 Cryptographic Functionality

3.1.4.1 Cryptographic Operation

The platform provides the application with *encryption and decryption* functionality as specified in *FIPS 197 (AES)* [5] for key length *128 or 256 bit* and modes *ECB and CBC, CTR and GCM*.

The platform provides the application with *encryption and decryption* functionality as specified in *NIST SP800-67 Rev. 2 (TDEA)* [6] for key length *112 or 168 bit* and modes *ECB and CBC and CTR*.

The platform provides the application with *hashing* functionality as specified in *FIPS 180-4* [4] for digests of *160 bits (SHA-1), 224bit (SHA-224) and 256bit (SHA-256)..*

The support for cryptographic operations is described in the Security Reference Manual*.*

The Cryptographic Acceleration and Assurance Module (CAAM) provides hardware acceleration for the AES and SHA operations.

The Cryptographic Acceleration and Assurance Module (CAAM) includes local storage in which keys can be stored and can then be used for cryptographic computations without ever being readable from the application. An OTP key is also stored in eFuses; it cannot be read by the application and it is copied directly into the CAAM during its initialization. This key can be used as a Key Encryption Key (KEK) to protect other cryptographic keys or sensitive credentials.

The cryptographic functionalities are tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.4.2 Cryptographic Keystore

The platform provides the application with a way to store *cryptographic keys* such that not even the application can disclose this data. This data can be used for the cryptographic operations: *encryption, decryption, signature generation*.

The Cryptographic Acceleration and Assurance Module (CAAM) includes local storage in which keys can be stored and can then be used for cryptographic computations without ever being readable from the application. An OTP key is also stored in eFuses; it cannot be read by the application and it is copied directly into the CAAM during its initialization. This key can be used as a Key Encryption Key (KEK) to protect other cryptographic keys or sensitive credentials.

The CAAM is tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.4.3 Cryptographic Random Number Generation

The platform provides the application with a way based on *physical noise* to generate random numbers to as specified in SP800-90B [7].

The platform includes a Standalone True Random Number Generator (SA-TRNG) module that generates a 512-bit entropy as needed by an entropy-consuming module or by other post-processing functions.

The RNG functionality is tested against a defined stochastic model by means of simulation tests during the design phase and by validation campaigns before chip

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release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.1.5 Compliance Functionality

3.1.5.1 Secure Encrypted Storage

The platform ensures that all data stored by the application, with the exception of *data that the user doesn't explicitly encrypt*, is encrypted as specified in *FIPS 197 (AES)* [5] with a platform instance unique key of keylength *128* in *ECB or CTR* modes.

An OTP key is stored in eFuses and used in the CAAM; it cannot be read by the application and it is copied directly into the CAAM during its initialization. This key can be used as a Key Encryption Key (KEK) to protect other cryptographic keys or sensitive credentials.

The On-The-Fly AES Decryption (OTFAD) module provides an advanced hardware implementation that minimizes any incremental cycles of latency introduced by the decryption in the overall external memory access time. The OTFAD engine also includes complete hardware support for a standard AES key unwrap mechanism to decrypt a key BLOB data instruction containing the parameters needed for up to 4 unique AES contexts.

The secure storage functionalities are tested thoroughly by means of simulation tests during the design phase and by validation campaigns before chip release. Each die undergoes production tests to ensure its correct functioning on each final product.

3.2 Security Assurance Requirements

The claimed assurance requirements package is: **SESIP1** as defined in [1]. The assurance requirements are as follows:

Table 3. Security Assurance Requirements for SESIP1

Assurance Class	Assurance Families
ASE: Security Target Evaluation	ASE_INT.1 ST Introduction ASE_OBJ.1 Security requirements for the operational environment ASE_REQ.3 Listed security requirements ASE_TSS.1 TOE summary specification
ALC: Life-cycle Support	ALC_FLR.2 Flaw reporting procedures

3.2.1 Flaw Reporting Procedures (ALC_FLR.2)

In accordance with the requirement for flaw reporting procedures (ALC_FLR.2), the developer has defined the following procedure:

NXP has defined a Product Security Incident Response Process (PSIRP), implemented by a dedicated team (PSIRT). This process provides a publicly available interface (https://nxp.com/psirt), and includes 4 steps:

• **Reporting**. The process begins when the PSIRT becomes aware of a potential security vulnerability in an NXP product. The reporter receives an acknowledgment and updates throughout the handling process.

• **Evaluation**. The PSIRT confirms the potential vulnerability, assesses the risk, determines the impact and assigns a processing priority. If the vulnerability is

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confirmed, the priority determines how the issue is handled throughout the remaining steps in the process.

- **Solution**. Working with PSIRT, the product team develops a solution that mitigates the reported security vulnerability. Solutions will take different forms based on the vulnerability. Because of the nature of NXP products – mostly silicon products where the firmware is in ROM -, very often the solution can only be provided in a next version of the chips and the short-term solution will consist of recommending security measures to be applied in systems using the NXP product.

- **Communication**. As said above, because of the nature of the NXP products, the solution to systems using the affected products often needs to be found in additional countermeasures in those systems. The communication on the vulnerability and solutions will in most cases be done directly towards the affected customers. For previously unknown or unreported issues, NXP will acknowledge the reporter of the issues (unless the reporter requests otherwise).

The firmware located in the on-chip ROM of the platform cannot be updated or patched. However, the platform's High Assurance Boot (HAB) feature is able to verify the authenticity of customer code during the initial boot and outside of the boot sequence, providing an appropriate mechanism for supporting the update of this code. The update mechanism itself has to be provided by the customer, most likely at the operating system level and is not in scope of this evaluation.

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4 Mapping and Sufficiency Rationales

4.1 ITP1 Sufficiency

Assurance Class	Assurance Familiy	Covered By	Rationale
ASE: Security Target Evaluation	ASE_INT.1 ST Introduction	Section 1	The ST reference is in Section 1.1, the TOE reference in Section 1.2, the TOE overview and description in TOE Overview and Description.
	ASE_OBJ.1 Security requirements for the operational environment	Section 2	The objectives for the operational environment in Section 2 refer to the guidance documents.
	ASE_REQ.3 Listed security requirements	Section 3	All SFRs in this ST are taken from [1]. SFR "Identification of Platform Type" is included. SFR "Secure Update of Platform" is mentioned but refers to ALC_FLR.2.
	ASE_TSS.1 TOE Summary Specification	Section 3	All SFRs are listed per definition, and for each SFR the implementation and verification is defined in the SFR.
ALC: Life-cycle Support	ALC_FLR.2 Flaw reporting procedures	Section 3.2.1	The flaw reporting and remediation procedure is described.

5 Bibliography

5.1 Evaluation Documents

[1]   Security Evaluation Scheme for IoT Platforms, Version 1.1.

5.2 Developer Documents

[2]   i.MX 7ULP Applications Processor Reference Manual 2.0, NXP Semiconductors, Document Number: IMX7ULPRMV2.

[3]   i.MX 7ULP 2.0 Security Reference Manual, NXP Semiconductors, Document Number: IMX7ULPSRMV2.

5.3 Standards

[4]   FIPS PUB 180-4: Secure Hash Standard (SHS), Federal Information Processing Standards Publication, Information Technology Laboratory, National Institute of Standards and Technology, August 2015.

[5]   FIPS PUB 197: Advanced Encryption Standard (AES), Federal Information Processing Standards Publication 197, US Department of Commerce/National Institute of Standards and Technology, 26 November 2001.

[6]   NIST SP 800-67, Recommendation for the Triple Data Encryption Algorithm (TDEA) Block Cipher, revised January 2012, National Institute of Standards and Technology.

[7]   NIST SP 800-90B, Recommendation for the Entropy Sources Used for Random Bit Generation, National Institute of Standards and Technology, January 2018.

[8]   PKCS #1: RSA Cryptography Standard, Version 2.2, October 27, 2012, RSA Laboratories

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